Parallel Numerical Algorithms

Chapter 1 – Parallel Computing

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CS 554 / CSE 512

Outline

1. Motivation
2. Architectures
   - Taxonomy
   - Memory Organization
3. Networks
   - Network Topologies
   - Graph Embedding
   - Topology-Awareness in Algorithms
4. Communication
   - Message Routing
   - Communication Concurrency
   - Collective Communication

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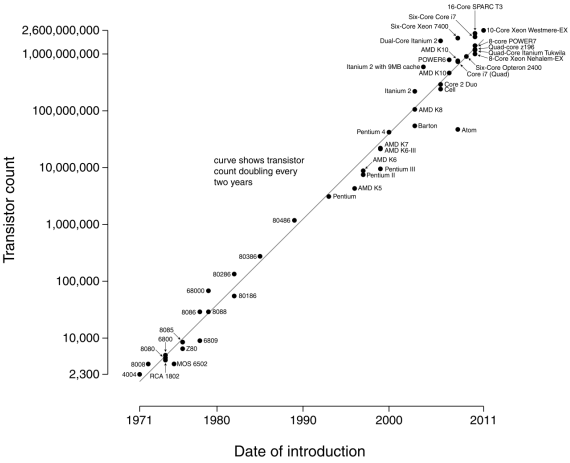
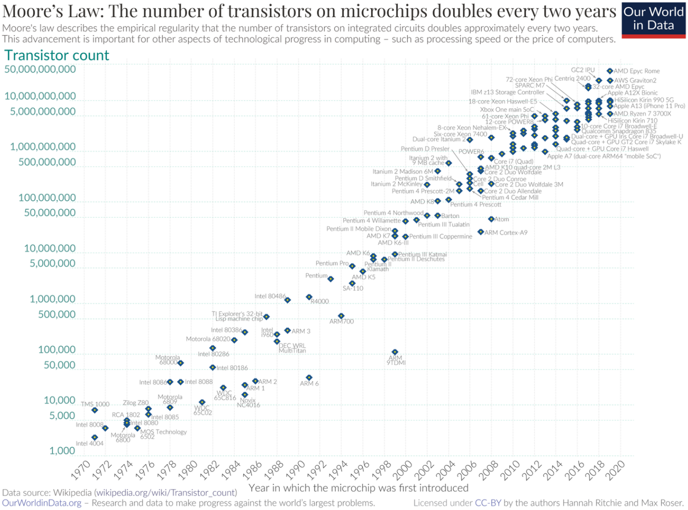
- Nevertheless, clock speed did in fact double every two years from roughly 1975 to 2005, but has now flattened at about 3 GHz due to limitations on power (heat) dissipation

Moore's Law

Microprocessor Transistor Counts 1971-2011 & Moore's Law



Moore’s Law, Architectures through 2020



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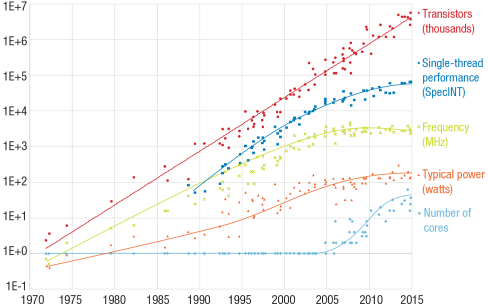
Dennard scaling: power usage scales with area, so Moore's law enables higher frequency with little increase in power



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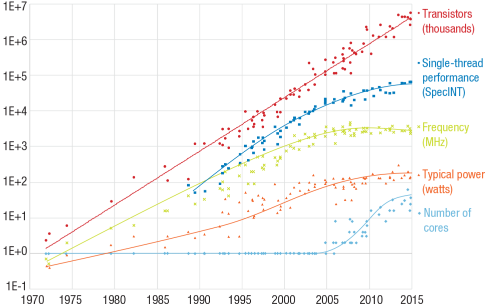

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- so can no longer increase frequency without increasing power, must add cores or other functionality

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- Nevertheless, to attain extreme levels of performance (petaflops and beyond) necessary for large-scale simulations in science and engineering, many processors (often thousands to hundreds of thousands) must work together in concert
- This course is about how to design and analyze efficient numerical algorithms for such architectures and applications

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  - general purpose parallel computers

SPMD Programming Style

SPMD (single program, multiple data): all processors execute same program, but each operates on different portion of problem data

- Easier to program than true MIMD, but more flexible than SIMD
- Although most parallel computers today are MIMD architecturally, they are usually programmed in SPMD style

Architectural Issues

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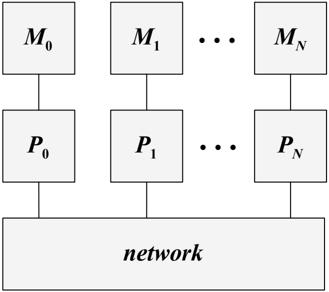
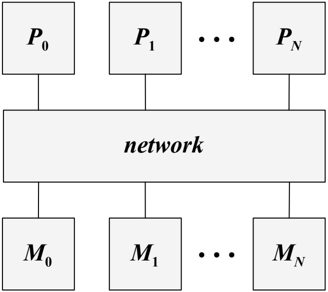
- *interconnection network* : topology, switching, routing?

Distributed-Memory and Shared-Memory Systems



distributed-memory multicomputer



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- Limited connectivity necessitates routing data through intermediate processors or switches

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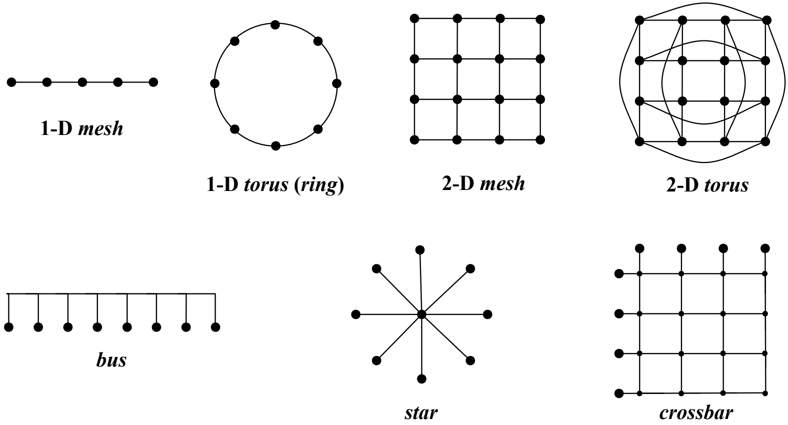

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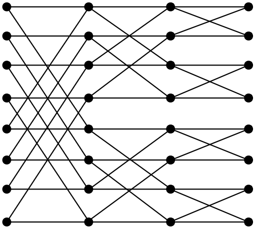
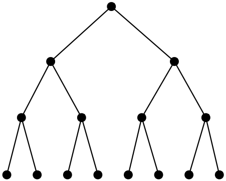


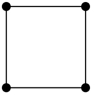
butterfly



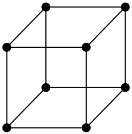
binary tree

0-*cube*

1-*cube*



2-*cube*



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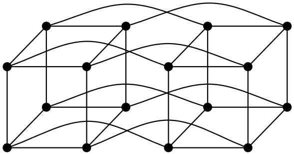

4-*cube*

hypercubes

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- *Spanning tree*: subgraph that includes all nodes of given graph and is also a tree

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- *Distance* between two nodes: number of edges (*hops*) in *shortest* path between them

Network Properties

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- *edge length*: maximum physical length of any wire; may be constant or variable as number of processors varies

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3-D torus	k^3	6	$3k/2$	$2k^2$	const

Network Properties

Network	Nodes	Deg.	Diam.	Bisect. W.	Edge L.
bus/star	$k+1$	k	2	1	var
crossbar	k^2+2k	4	$2(k+1)$	k	var
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2-D mesh	k^2	4	$2(k-1)$	k	const
3-D mesh	k^3	6	$3(k-1)$	k^2	const
n-D mesh	k^n	$2n$	$n(k-1)$	k^{n-1}	var
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hypercube	2^k	k	k	2^{k-1}	var
butterfly	$(k+1)2^k$	4	$2k$	2^k	var

Graph Embedding

Graph embedding: $\phi\colon V_s \to V_t$ maps nodes in source graph $G_s = (V_s, E_s)$ to nodes in target graph $G_t = (V_t, E_t)$. Edges in G_s are mapped to paths in G_t.

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- *load*: maximum number of nodes in V_s mapped to same node in V_t
- *congestion*: maximum number of edges in E_s mapped to paths containing same edge in E_t
- *dilation*: maximum distance between any two nodes $\phi(u), \phi(v) \in V_t$ such that $(u, v) \in E_s$

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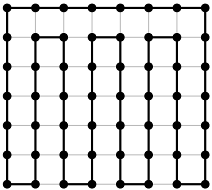
- Perfect embedding has load, congestion, and dilation 1, but not always possible
- Optimal embedding difficult to determine (NP-complete, in general), so heuristics used to determine good embedding

Examples: Graph Embedding

For some important cases, good or optimal embeddings are known, for example



ring in 2-D mesh

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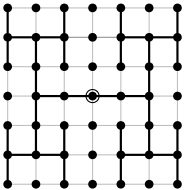
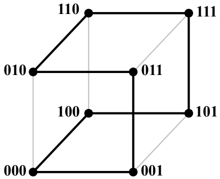


binary tree in 2-D mesh

dilation $\lceil (k-1)/2 \rceil$



ring in hypercube

dilation 1

Gray Code

Gray code : ordering of integers 0 to $2^k - 1$ such that consecutive members differ in exactly one bit position

Example: binary reflected Gray code of length 16

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$0001 = 1$		$1101 = 13$
$0011 = 3$		$1111 = 15$
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- For mesh or torus of higher dimension, concatenating Gray codes for each dimension gives embedding in hypercube
- Hypercubes provide an effective paradigm for low-diameter target network in designing parallel algorithms

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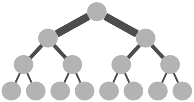

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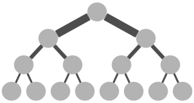

  - When increasing processors, bisection bandwidth scales with $O(p^{2/3})$ as opposed to $O(1)$ for binary trees

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- The Slim Fly network yields degree of roughly $\sqrt{p}$

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- Nevertheless, topologies provide a convenient visual model for design of parallel algorithms

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- A good parallel algorithm design methodology is to
  1. try to obtain cost-optimality for a fully-connected network
  2. organize it so it achieves the same cost on some network topology that is as sparsely-connected as possible

Message Passing

Simple model for time required to send message (move data) between adjacent nodes:

$$T_{\text{msg}} = \alpha + \beta\,\mathrm{s}$$

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For real parallel systems $\alpha \gg \beta$, so we often simplify $\alpha + \beta \approx \alpha$

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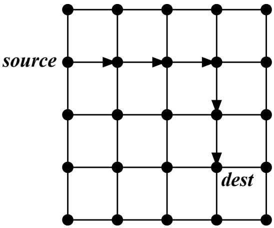
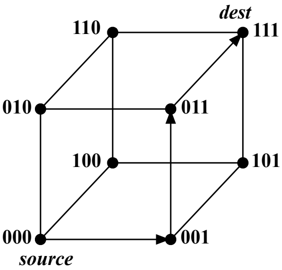
- *circuit switched* or *packet switched*, depending on whether entire message goes along reserved path or is transferred in segments that may not all take same path

Message Routing

Most regular network topologies admit simple routing schemes that are static, deterministic, and minimal



2-D mesh



hypercube

Store-and-Forward vs. Cut-Through Routing

Store-and-forward routing: entire message is received and stored at each node before being forwarded to next node on path, so

$$T_{\text{route}} = (\alpha + \beta \mathrm{s})D, \text{ where } D = \text{distance in hops}$$

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Generally $t_h \leq \alpha$, so we can treat both as network latency,

$$T_{\text{route}} = \alpha D + \beta \text{s}$$

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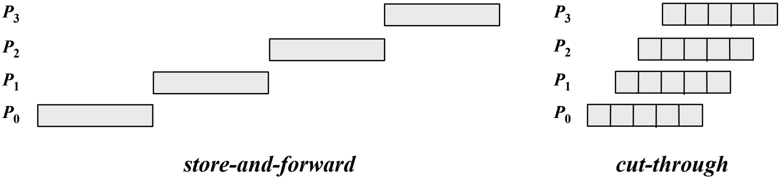

Cut-through (wormhole) routing greatly reduces distance effect, but aggregate bandwidth may still be significant constraint

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- *One-to-All*: Broadcast, Scatter
- *All-to-One*: Reduce, Gather
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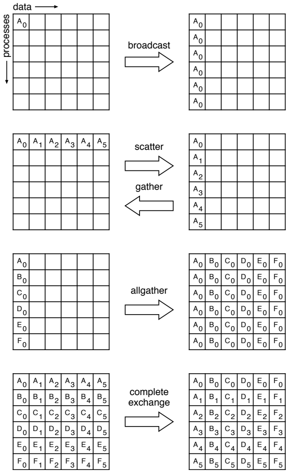
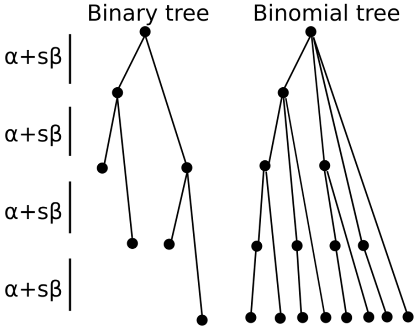
MPI (Message-Passing Interface) provides all of these as well as variable size versions (e.g. (All)Gatherv, All-to-allv).

Collective Communication



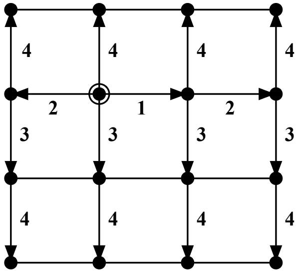
Broadcast

Broadcast: *source* node sends same message of size s to each of $p-1$ other nodes

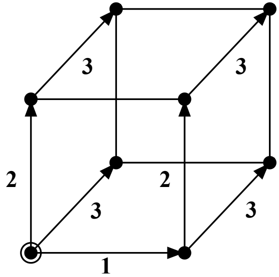


Binary or binomial trees are often used for one-to-all collectives like broadcast, but any spanning tree will do

Broadcast



2-D mesh



hypercube

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Cost of broadcast depends on network, for example

- 1-D mesh: $T = (p - 1)\,(\alpha + \beta \mathrm{s})$

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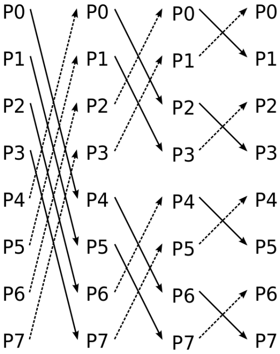
For long messages, bandwidth utilization may be enhanced by breaking message into segments and either

- *pipeline* segments along *single* spanning tree, or
- send each segment along *different* spanning tree having *same* root

For example, hypercube with 2^k nodes has k *edge-disjoint* spanning trees for any given root node

Butterfly Protocols

All collective-communication can be done near-optimally with *butterfly protocols*, which use all links of a hypercube network



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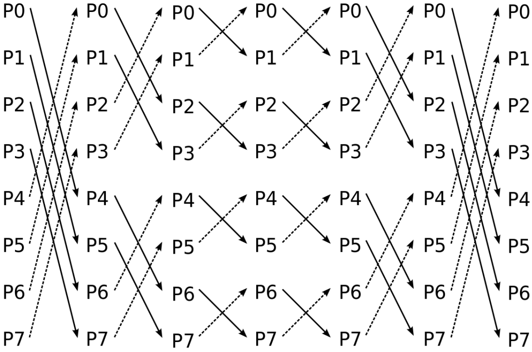
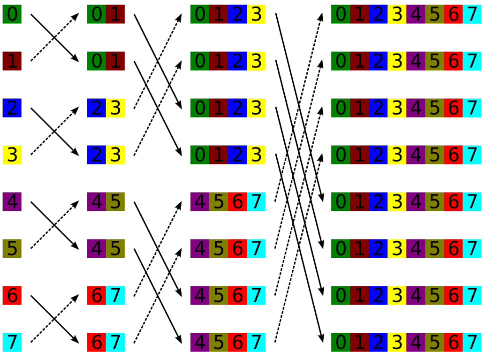


Butterfly Allgather (Recursive Doubling)

Allgather: each of p nodes sends message to all other nodes



Cost of Butterfly Allgather

The butterfly has $\log_2(p)$ levels. The size of the message doubles at each level until all s elements are gathered, so the total cost is

$$T_{\text{allgather}}(s,p) = \begin{cases} 0 & : p = 1 \\ T_{\text{allgather}}(s/2, p/2) + \alpha + \beta(s/2) & : p > 1 \end{cases}$$

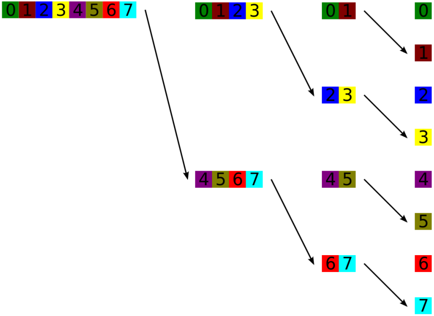
$$\approx \alpha \log_2(p) + \sum_{i=1}^{\log_2(p)} \beta s/2^i$$

$$\approx \alpha \log_2(p) + \beta s$$

The geometric summation in the cost analysis is typical for butterfly protocols for one-to-all and all-to-one collectives

Butterfly Scatter

Scatter: *source* node sends message of size s/p to each of $p - 1$ other nodes



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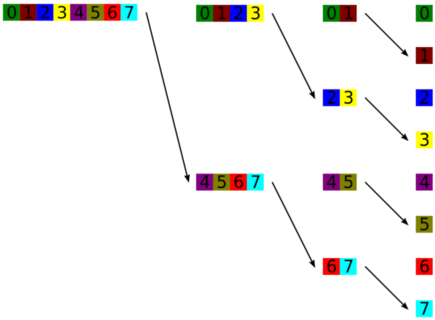
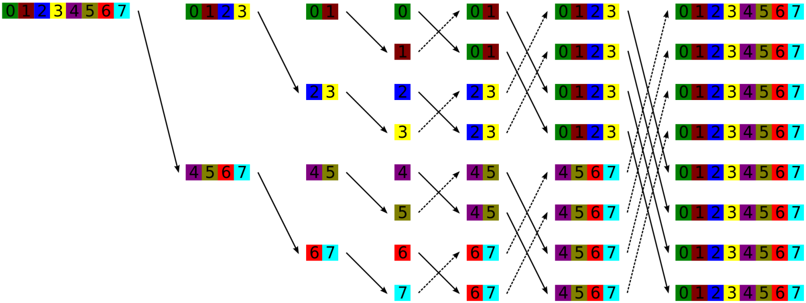


Note that the messages are forwarded down a binomial and not a binary spanning tree of nodes.

Butterfly Broadcast



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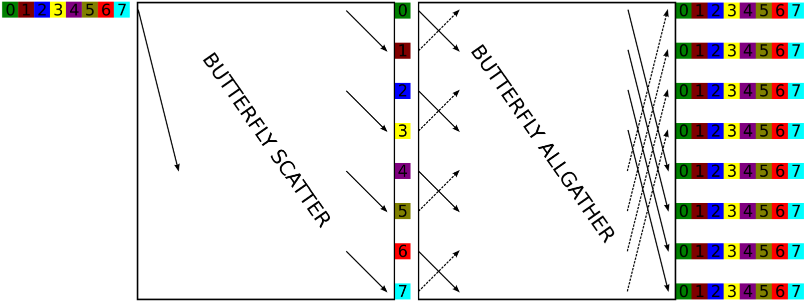

$$T_{\text{broadcast}} = T_{\text{scatter}} + T_{\text{allgather}} = 2T_{\text{allgather}}$$

Reduction

Reduction : data from all p nodes are combined by applying specified associative operation $\oplus$ (e.g., sum, product, max, min, logical OR, logical AND) to produce overall result

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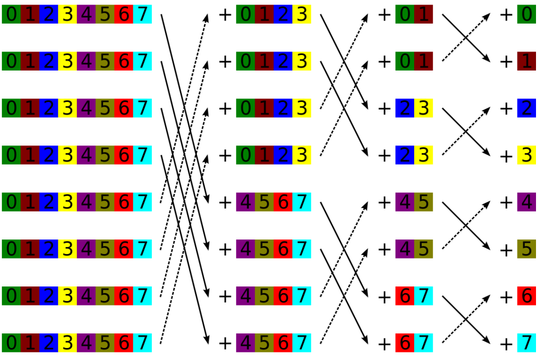
These one-to-all + all-to-one collectives have butterfly protocols with equivalent cost.

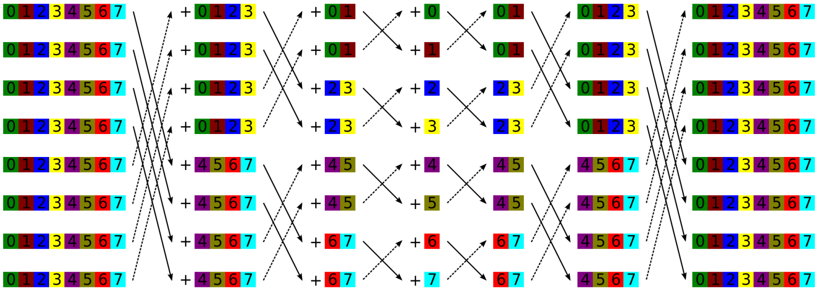
Butterfly Reduce-Scatter (Recursive Halving)

Reduce-scatter: a reduction with the result *distributed* over all p nodes

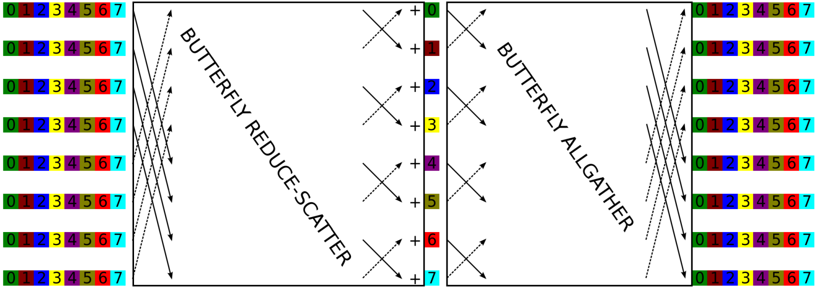


Butterfly Allreduce

Allreduce: a reduction with the result *replicated* on all p nodes

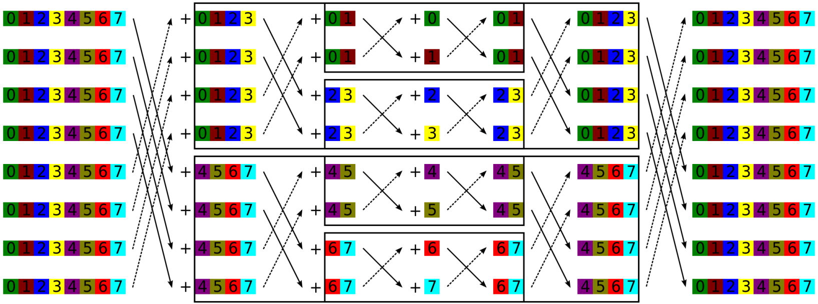


Butterfly Allreduce



$$T_{\text{allreduce}} = T_{\text{reduce-scatter}} + T_{\text{allgather}}$$

Butterfly Allreduce: note recursive structure of butterfly



Scan or Prefix

Scan or *prefix*: given data values $x_0, x_1, \ldots, x_{p-1}$, one per node, along with associative operation $\oplus$, compute sequence of partial results $y_0, y_1, \ldots, y_{p-1}$, where

$$y_k = x_0 \oplus x_1 \oplus \cdots \oplus x_k,$$

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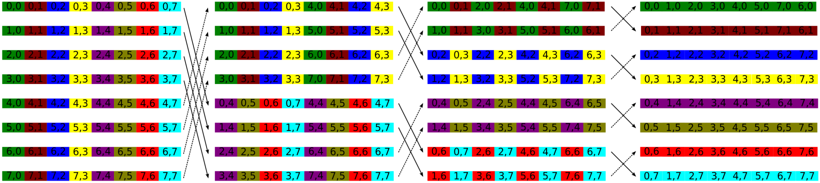
Scan can be implemented via a butterfly protocol similar to Allreduce, except intermediate results must be stored while doing recursive halving to be recombined when doing recursive doubling

Butterfly All-to-All



The size of the message stays the same at each level, so

$$T_{\text{all-to-all}}(s, P) = \qquad = \alpha \log_2(P) + \beta s \log_2(P)/2$$

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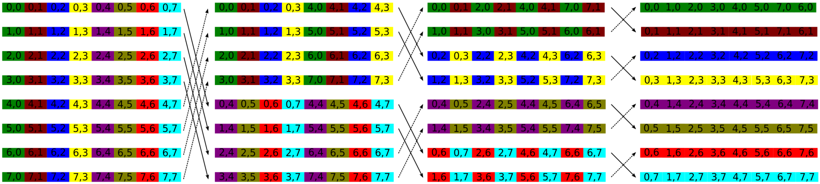

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Its possible to do All-to-All in less bandwidth cost (as low as βs by sending directly to targets) at the cost of more messages (as high as αP if sending directly)

Collectives on Mesh and Torus Networks

Butterfly protocols cannot be mapped to tori without dilation

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- all-to-all cost generally depends on the bisection bandwidth of the network (proportional to $p^{(d-1)/d}$ for d-dimensional torus/mesh)

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